Rules of FPGA Hackathon on-line

Version 2.0

FPGA Hackathon on-line

21-22 November 2020

Contents

The FPGA Hackathon on-line ("**Hackathon**") is a contest organized by **Nokia Solutions and Networks Sp. z o.o.** with its registered office in Warsaw, address: ul. Rodziny Hiszpańskich 8, 02-685, Warszawa, entered to the Register of Entrepreneurs of the National Court Register maintained by the District Court for the Capital City of Warsaw in Warsaw, 13th Division of the National Court Register under KRS number 0000265262, NIP 113-26-39-219, REGON 140718341, share capital of 27 209 000,00 PLN ("**Organizer**", "**Nokia**"). Individuals and teams participating in the FPGA (individually, "**Contestant**"; collectively, "**Contestants**") are invited to develop ideas and applications based on the FPGA goals and information provided by the Organizer. Participation is entirely voluntary and free of charge. The Organizer will not compensate any Contestant for time spent or tasks performed while participating in the FPGA .

Only those teams invited into the FPGA are permitted to join the event as Contestants.

For matters not covered by these Rules of FPGA Hackathon on-line ("**Rules of Hackathon**"), the **Regulations governing participation in free on-line events** ("**Regulations**") issued by Nokia Solutions and Networks Sp. z o.o. shall apply.

The Hackathon is held on **21-22 November 2020**, and is preceded by FPGA Conference. The registration process for on-line FPGA Conference is separate from registration process for FPGA Hackathon. Detailed information is available at fpgahackathon.com.

1 Definitions

"**Affiliate**" means an entity:

(i) which is directly or indirectly controlling Nokia Solutions and Networks Oy;

(ii) which is under the same direct or indirect ownership or control as such Nokia Solutions and Networks Oy; or

(iii) which is directly or indirectly owned or controlled by Nokia Solutions and Networks Oy.

For these purposes, an entity shall be treated as being controlled by another if that other entity has fifty percent (50 %) or more of votes in such entity, is able to direct its affairs and/or to control the composition of its board of directors or equivalent body.

"**API**" means application programming interface which is a set of functions and procedures that allow the creation of applications which access the features or data of an operating system, application, or other service.

"**Challenge Website**" means **fpgahackathon.com**

"**Intellectual Property Rights**" or "**IPR**" means all intellectual property and proprietary rights, registered or unregistered throughout the world, including:

(i) patents, copyright (including software), registered designs, trademarks, trade secrets, other proprietary rights, semi-conductor or circuit layout right, know-how, inventions and the right to have confidential information kept confidential; and

(ii) any application or right to apply for registration of any of the rights referred to in paragraph (a) above.

"**Prize**" means the award(s) set out in the Challenge Website but excludes any bonus prizes that may be awarded by the Organizer at its discretion.

2 Organizers

This competition is organized by the Organizer. The Organizer may engage its Affiliates and other stakeholders to facilitate the competition, such as challenge partners, technology and coaching enablers.

The entity that issues and settles the Prizes is iMedius Sp. z o.o. , Mogilska 69, 31-545 Kraków, entered to the Register of Entrepreneurs of the National Court Register maintained by the District Court for Kraków-Downtown in Cracow, 11th Division of the National Court Register under KRS number 0000112811, NIP: 6751196797, REGON: 35155369, share capital of 200 000,00 PLN.

The sponsor of the prizes is Intel Technology Poland Sp. z o.o., Słowackiego 173, 80-298 Gdańsk, entered to the Register of Entrepreneurs of the National Court Register maintained by the District Court in Gdańsk, 12th Division of the National Court Register under KRS number 0000101882, NIP 9570752316, REGON 191879099, share capital of 200 000,00 PLN.

3 FPGA Format and Schedule

The timelines for the FPGA FPGA are visible in the event schedule specified in the Challenge Website. Deadlines for Teams registrations is 16 November 2020. All Contestants must confirm their registration individually by the deadline to be eligible to participate in the FPGA FPGA as a team.

The challenge for FPGA Hackathon will be presented according to the schedule on the first day of event.

During the Event Organizers will provide:

- access to setup with development board (Cyclone V GX Starter Kit),
- access to selected FPGA Design and Verification related tools under provided licenses:
  - Matlab & Simulink from MathWorks,
  - Questa Simulator from Mentor Graphics,
  - OneSpin Formal Verification tools from Onespin,

- Quartus from Intel,
- Active-HDL from Aldec.

With given assets, Contestants relying on their knowledge and chosen technology are supposed to submit solution on assigned GitLab repository for task announced at hackathon day. Solution should contain whole Quartus project needed to bitfile generation (including all configuration files and HDL code). Participants are forbidden to change given modules configuration."

When challenge is resolved and developed to a stage where it is a usable solution to one or more of the issues and/or goals set forth by the Organizer, the Contestants submit their submissions to the Organizer for review ("**Submission**"). For clarity, the term Submission is not limited to software applications, but includes any solution or application which can be applied to the issues and/or goals set by the Organizer for the competition.

The specific technical requirements are published on Challenge Website and includes, but are not limited to:

- installed SSH client (e.g Putty),
- installed VNC (e.g. TigerVNC),
- creating Discord account using registration link provided in e-mail sent by Organizer.

Winners will be selected after the conclusion review of all Submissions.

4 Registration process

4.1 General eligibility requirements for all Contestants

Participants of the Hackathon may only be adults with full legal capacity.

The following individuals are NOT eligible to participate in the FPGA as Contestants, regardless of whether they meet other eligibility criteria:

- employees of the Organizer or its Affiliates or any individual who at the time of the FPGA is involved with the design, production, or execution of the FPGA , including each member of any such individual's immediate family or household; and
- any individual whose participation in the FPGA would, in the determination of the Organizer or its Affiliates, create a conflict of interest.

Members of an individual's immediate family include individual's spouse, children and step-children, parents and step-parents, and siblings and step-siblings; and

Members of an individual's household include any other person that shares the same residence as such individual for at least three (3) months of the year.

4.2 Specific eligibility requirements for all Contestants

Each team shall appoint one individual (Team leader) to represent and act on behalf of the Team, including fulfilling registration form and entering the Submission.

Team Leader has to register whole Team of 2-3 members by providing: name, surname and e-mail address of each of Team member. Additionally, Team Leader has to provide his/her telephone number. Each Team member will receive e-mail with link to individual registration in order to confirm participation and give appropriate information and consents. Team will be successfully registered only after receiving required consents and statements from all Team members.

The number of Contestants is limited. The limit is 100 people. Registered team is accepted by Organizer, based on information about Team, which is provided during registration in field “Why your Team should be qualified for the Event?”.

4.3 General Registration Requirements

Each Contestant is responsible for acquiring the necessary rights to participate in the FPGA . These rights include but are not limited to, licenses and permission to participate in the challenge from the Contestant’s employer.

For clarity, Organizer shall NOT be responsible for any expenses incurred by Contestant for participating in the FPGA or associated with the use of any programs used to create the Submission, subject to software made available by Organizer and determined at Challenge Website.

4.4 Registration Requirements

The registration process of each Contestant requires the acceptance of all the terms and conditions of these Rules of Hackathon, Regulations, Nokia Privacy Policy and granting consents for the processing of personal data.

Hackathon will take place by means of using Discord service and the Contestant is required to become acquainted with and accept the Discord Terms of Service during registration process.

The Contestant acknowledges that the FPGA Hackathon is recorded by the Organizer for the purpose of promoting, informing, and reporting on the Event. In the course of the registration process, the Contestant is requested to express their consent to the use of their image, voice, chat content, and identification data (nick, login), recorded during the Hackathon in the form of videos and recordings, and to their dissemination by the Organizer. Consent includes such forms of dissemination as: availability at www.nokia.com, nokiakrakow.pl, social media (Facebook, LinkedIn, YouTube), promotional and information materials for the purposes of promoting, informing, and reporting on the Hackathon. Consent applies to multiple, unlimited by time and

territory, dissemination of an image, voice, chat content and identification data (nick, login), recorded during the Hackathon.

The Hackathon may be attended by persons who have received an invitation (enrolment confirmation) from the Organizer to the specified e-mail address provided during the registration process.

The number of Contestants is limited.

5 Language Requirements

Submission materials must be in English.

6 General Requirements for Submissions

The Submission may utilize code, works, rights, APIs and data from third parties, provided the Contestant has obtained written permission, license and/or any other necessary rights from such third parties to use such code, works, rights, APIs or data in the manner utilized by the Submission.

Submissions must not violate any applicable law or regulation; depict hatred; be in bad taste or be derogatory towards any person or group of persons or any race, ethnic group or culture; threaten a specific community in society(including any specific race, ethnic group or culture); incite violence or be likely to incite violence; contain vulgar or obscene language or excessive violence; contain pornography, obscenity or sexual material or activity; or disparage third parties or the Organizer or anyone involved in organizing or supporting the FPGA . Organizer reserves the right to reject any Submission at any time during the FPGA that it deems to be in violation of these requirements.

Contestant must not attempt to intentionally duplicate the Submission of another Team. The Organizer reserves the right in its sole discretion to disqualify any Submission that is an exact or substantially similar duplicate of another Submission.

Submissions must not contain any software routine, code, or instruction, hardware component or combination of the foregoing which:

- permits unauthorized access to Organizer’s IT network or Organizer’s Confidential Information,
- or can disable, delete, modify, damage or erase software, hardware or data or otherwise cause an information security risk.

Submissions may include third party open source and/or proprietary code not produced by the Contestant if such code is available to the public free of charge or for a nominal fee. Any open

source and/or proprietary code must be identified and the Contestant must follow applicable licensing conditions for such code.

The Organizer may determine on Challenge Website available software of Organizer, Organizer's Affiliates or Organizer's partners made available for the purposes of Submission during Hackathon.

Submissions may not violate the Intellectual Property Rights or any other rights of any other person or entity.

Contestants must not state or otherwise imply endorsement of their Submission by the Organizer in any of the Submission components.

By entering a Submission, each Contestant represents and warrants that:

(i) the Submission does not contain any software routine, code, or instruction, hardware component or combination of the foregoing which:
    a. permits unauthorized access to Organizer's IT network or Organizer's Confidential Information; or
    b. can disable, delete, modify, damage or erase software, hardware or data;
(ii) the Submission is free from any claim of infringement of any copyright, trademark, trade secret, patent or other proprietary right of any third party; and
(iii) Organizer's receipt and use of the Submission does not and shall not infringe any copyright, trademark, patent or other proprietary right of any third party or constitute the wrongful taking of any third party's proprietary or confidential data or trade secret.

7 Winner Selection and Judging Criteria

All eligible Submissions will be judged by a panel of judges (the "**Judges**") selected by the Organizer. The FPGA has 2-5 judges per track with expertise in their tracks' field. The Organizer reserves the right to substitute or modify the judging panel at any time for any reason.

All Judges shall be impartial, fair and reasonable. Any Judge may excuse him or herself from judging a Submission if the Judge or the Organizer considers that it is inappropriate, for any reason, for the Judge to evaluate a specific Submission or group of Submissions. A Contestant's likelihood of winning will depend on various criteria set forth below, and the number and quality of all the Submissions.

8 General Evaluation Criteria for Submissions

8.1 Main criteria

Submited Quartus project should allow bitfile generation. Generated bitfile will be automatically verified at setup containing two Cyclon V kits by using script created in Python3. Script result is the measurement of required performance factor (announced during Hackathon task presentation) which is base for winners ranking.

Organizer will check the best 3 solutions manually to confirm that configuration files are not modified by participants. In case of proven modifications team will be disqualified.

8.2 Additional criteria

Additional more detailed criteria might be defined at Challenge Website.

9 Verification of Potential Winners

ALL POTENTIAL FPGA FPGA WINNERS ARE SUBJECT TO VERIFICATION OF IDENTITY, QUALIFICATIONS AND ROLE IN THE CREATION OF THE SUBMISSION BY THE ORGANIZER. ORGANIZER'S DECISIONS ARE FINAL AND BINDING IN ALL MATTERS RELATED TO THE HACKATHON. Potential winners must continue to comply with all terms and conditions of these Rules of Hackathon throughout the FPGA FPGA .

Source code must be submitted for verification audit by an independent third party if the Submission is under suspicion for fraud, breach of these Rules of Hackathon or any violation of third party Intellectual Property Rights (all information will be held confidential by Nokia and the auditor).

At the sole discretion of the Organizer, a potential winner will be deemed ineligible to win if such potential winner refuses the Prize or the Submission or the Contestant is disqualified for other reason.

In the event of such disqualification, the Organizer, in its sole discretion, may award the applicable Prize to another Contestant. The disqualification of one (or more) team members from further consideration in the FPGA for any reason may result in the disqualification of the entire team, as determined by the Organizer in its sole discretion.

10 Prizes

All prizes will be decided by the Judges consisting of Organizer's employees, partners' experts and/or external independent professionals. The list of Prizes will be published at the Challenge Website and the Organizer reserves the right to alter the list.

The Prize consists of an in-kind and if applicable also cash Prize, which will cover the income tax payable on in-kind Prizes. The Organizer reserves the right to withhold a portion of the cash Prize amount to comply with the tax laws of Poland. In-kind Prizes will not be exchanged for other Prizes or will not be exchanged for their cash equivalent.

The list of Prizes:

1st prize: 3x Intel NUC– estimated cost $350 per one item plus adequate cash prize covering the income tax (one awarded to each member of the team).

2nd prize: 3x Terasic Development Kit DE10-Nano Kit - $120 per one item plus adequate cash prize covering the income tax (awarded to each member of the team).

3rd prize: 3x Intel Neural Compute Stick – cost around $100 per one item plus adequate cash prize covering the income tax (awarded to each member of the team).

Notwithstanding anything stated herein, the Organizer explicitly reserves the right not to award any or some of the Prizes if it deems, in its sole discretion, that the Submissions do not address the issues and/or meet the goals set for the FPGA by the Organizer.

No transfer or substitution of a Prize is permitted (except as agreed among team members), unless approved by the Organizer.

In the event a Prize winner's / potential Prize winner's employer has a policy that prohibits the awarding of a Prize to an employee, the Prize will be forfeited and an alternate potential winner may be selected by the Organizer at its sole discretion.

11 Entry Conditions and Release

Each Contestant hereby acknowledges and agrees that the relationship between the Contestant and the Organizer is not a confidential, fiduciary, or other special relationship, and that the Contestant's decision to provide a Submission to the Organizer for the purposes of this FPGA does not place the Organizer, its Affiliates or its agents, in a position that is any different from the position held by the members of the general public with regard to elements of the Contestant's Submission, except as specifically provided in these Rules of Hackathon.

By entering, each Contestant agrees to comply with and be bound by these Rules of Hackathon and the decisions of the Organizer and/or the FPGA Judges, which are binding and final in all matters relating to this FPGA ; and

Each Contestant agrees release, indemnify, defend and hold harmless the Organizer and its Affiliates and companies organizing or facilitating FPGA , the Judges, the Prize suppliers and any other organizations responsible for organizing, fulfilling, administering, advertising or promoting the FPGA , and all of their respective past and present officers, directors, employees, agents and representatives (hereafter the "**Released Parties**") from and against any and all claims, expenses, damages and liabilities (including reasonable attorneys' fees) arising from or related to the FPGA , including but not limited to, damages of any kind to persons and property, including but not limited to: defamation, slander, libel, violation of right of publicity; infringement of trademark, copyright or other Intellectual Property Rights; property damage, or death or personal injury arising out of or relating to a Contestant's entry in the FPGA , participation in the FPGA (including but not limited to the creation of a Submission or entry of a Submission); breach of any representations or warranties given by the Contestant; acceptance or use or misuse of a Prize ; and/or the use, copying, creation of derivative works, distribution, display and performance of a Submission as authorized by or licensed under these Rules of Hackathon.

12 General Conditions

The Organizer reserves the right to cancel, suspend and/or modify the FPGA , or any part of it, if any fraud, technical failure or any other unanticipated factor or factor beyond the Organizer's reasonable control impairs the safety, integrity or proper functioning of the FPGA , as determined by the Organizer in its sole discretion. The Organizer reserves the right in its sole discretion to disqualify any Contestant it finds to be tampering with the entry process, disturbing the operation of the FPGA or to be acting in violation of these Rules of Hackathon or Regulations or in a manner that is inappropriate, unsportsmanlike, not in the best interests of this FPGA , or a violation of any applicable law or regulation.

In the event of any discrepancy or inconsistency between the terms and conditions of the Rules of Hackathon and disclosures or other statements contained in any FPGA materials, including but not limited to the Challenge Website or any advertising (e.g. online ads), the terms and conditions of the Rules of Hackathon shall prevail.

In the event of any discrepancy or inconsistency between the terms and conditions of the Rules of Hackathon and Regulations, the terms and conditions of the Rules of Hackathon shall prevail.

The Organizer reserves the right, without liability, to amend the terms and conditions of the Rules of Hackathon at any time, including the rights or obligations of the Contestant and the Organizer. The Organizer will post the terms and conditions of the amended Rules of Hackathon on the

Challenge Website. Any such amendment will become effective at the time the Organizer posts the amended Rules of Hackathon, unless expressly stated otherwise in the amendment.

Excluding Submissions, all intellectual property related to this FPGA , including but not limited to trademarks, trade-names, logos, designs, promotional materials, web pages, source codes, drawings, illustrations, slogans and representations are owned or used under license by the Organizer. All rights are reserved by the Organizer and its licensors. Unauthorized copying or use of any copyrighted material or intellectual property without the express written consent of its owners is strictly prohibited.

Should any provision, in whole or in part, of these Rules of Hackathon be or become illegal or unenforceable in the jurisdiction of a permitted Contestant, such illegality or unenforceability shall leave the remainder of these Rules of Hackathon unaffected and valid. The illegal or unenforceable provision (or part thereof) shall be replaced by a valid and enforceable provision (or part) that comes closest and best reflects the Organizer's intention in a legal and enforceable manner with respect to the invalid or unenforceable provision (or part).

These Rules of Hackathon become effective on 15 October 2020.

13 Privacy

Organizer will handle the personal data in accordance with the Nokia Privacy Policy available at: http://www.company.nokia.com/privacy and the Regulations governing participation in on-line free events issued by Nokia Solutions and Networks Sp. z o.o. available at nokiakrakow.pl.

With regards to privacy, all Contestants must agree to below Privacy statement during registration to the Event:

"I hereby express my consent to the processing of my personal data provided in the attendance form for the purpose of registering and attending the FPGA Conference 2020 organised by Nokia Solutions and Networks Sp. z o.o., with its registered office in Warsaw, Poland pursuant to the Rules of FPGA Hackathon on-line, the Regulations governing participation in free on-line events and the Nokia Privacy Policy.

The Organizer has the right to send a weekly email newsletter to Contestants to keep them up to date on the FPGA . The Contestants can unsubscribe from this newsletter by using the link provided in such newsletters.

14 FPGA Results

FPGA Hackathon results are announced at the end of Hackathon during Results Presentation ceremony, according to schedule available at the Challenge Website.

Prizes will be granted to the winner teams during Awards Ceremony at the end of Hackathon and shipped to each winner Contestant individually.

If the winner Contestant fails to provide valid shipping address within 7 days of the end of hackathon are forfeited.

15 Contact Us

If you have any questions or wish to send us any notice regarding this FPGA , please email contact.hackathon@nokia.com